

# LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	7/12	Discrete time signals & systems	1			
2	8/12	Linear shift invariant systems	1			
3	9/12	Stability & Causality	1			
4	9/12	Linear Constant coefficient D.E	1			
5	14/12	Linear Constant coefficient D.E	1			
6	15/12	Solution for LCCDE	1			
7	16/12	freq. domain representation of discrete time systems	1			
8	16/12	Introduction to DFS	1			
9	21/12	Properties of DFS	1			
10	22/12	Properties of DFS	1			
11	23/12	Problems on DFS & DTFT	1			
12	23/12	DFS Representations of periodic sequences	1			
13	28/12	Definition of DFT	2			
14	29/12	Properties of DFT	2			
15	30/12	Proof of properties of DFT	2			
16	30/12	Linear convolution of seq. using DFT	2			
17	4/01	Computation of DFT	2			
18	5/01	Radix-2 decimation in time domain	2			
19	6/01	Decimation in freq. domain algorithm	2			
20	6/01	Inverse FFT	2			

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21	11/01	FFT for complex N	2			
22	18/01	Definition of ZT properties	2			
23	19/01	Roc, Inverse ZT	2			
24	20/01	Relation b/w FT and ZT applications	2			
25	20/01	Solution for diff equations of digital filter	3			
26	25/01	Block diagram representation of LCC DFE	3			
27	27/01	Block structure of HA Direct form, Indirect	3			
28	27/01	Cascade form, parallel form	3			
29	1/2	Lattice ladder structure, Transposition	3			
30	2/2	Analogue filter approx Butterworth, Chebyshev	3			
31	3/2	Bilinear transformation (Bilinear method)	3			
32	3/2	Design examples of IIR filters	3			
33	8/2	Block transformation (s to z domain) problem	3			
34	9/2	FIR digital filter Basic structure of FIR	4			
35	10/2	Direct form, Cascade form, frequency sample	4			
36	10/2	Lattice form Characterization of FIR	4			
37	15/2	freq. response of FIR digital filter	4			
38	16/2	Design of FIR digital filter using window method	4			
39	17/2	Freq sampling techniques	4			
40	17/02	Comparison of PAB, IIR digital filter	3, 4			

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41	22/2	Multirate digital signal processing.	4			
42	23/2	Decimation, Interpolation	4			
43	24/2	Sampling rate conversion	4			
44	24/2	Implementation of sampling rate conversion	4			
45	1/3	problems of FIR digital filters intro. tp	4			
46	2/3	problems of FIR digital filters using windows	4			
47	3/3	problems of FIR digital filters using windowing tech.	4			
48	8/3	Introduction to DSP processors	5			
49	9/3	Introduction to program- mable DSP	5			
50	10/3	Multiplexer and Accumulator (MAC)	5			
51	10/3	Modified bus structure	5			
52	15/3	Memory Access Schemes in DSP.	5			
53	16/3	Multiple access memory	5			
54	17/3	Multipoint memory	5			
55	17/3	VLSI Architecture	5			
56	22/3	Pipelining, Special Addressing modes	5			
57	23/3	on-chip peripherals	5			
58	24/3	Architecture of TMS320C5x - Intro	5			
59	24/3	Register file, CPU - (CALU)	5			
60	29/3	Accumulator, Arithmetic Registers,	5			

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61	30/3	Compare registers	5			
62	31/3	Block Move addr registers, PAU,	5			
63	31/3	Memory mapped registers, PC,	5			
64	5/4	some flags in the status registers	5			
65	6/4	on-chip registers on-chip peripheral	5			
66	7/4	Pipelining / special Addressing modes	5			
67	7/4	VLSI Architecture	5			
68	12/4	on-chip peripheral multiaccess memory.	5			
						8/30/12